What is claimed is:

1. A semiconductor-chip mounting substrate comprising:

a substrate having at least one projection thereon, which is integrally molded with said substrate;

a first bump obtained by forming a conductive layer on said projection; and

a semiconductor chip having a terminal projecting as a second bump on its surface;

wherein said semiconductor chip is mounted on said substrate such that said first bump contacts said second bump, and said semiconductor-chip mounting substrate comprises a pressure holding means for providing a required contact pressure between said first bump and said second bump.

2. The semiconductor-chip mounting substrate as set forth in claim 1, wherein said pressure holding means is a resin material filled and cured in a space between said substrate and said semiconductor chip.

3. The semiconductor-chip mounting substrate as set forth in claim 2, wherein said resin material has a coefficient of linear expansion greater than a material of said substrate.

4. The semiconductor-chip mounting substrate as set forth in claim 3, wherein a difference in the coefficient of linear expansion between said resin

material and the material of said substrate is in a range of 5×10^{-6} / °C to 60 $\times 10^{-6}$ / °C.

5. The semiconductor-chip mounting substrate as set forth in claim 1, wherein a surface roughness (Ra) of at least a top surface of said first bump is in a range of 0.1 to 3 μm.

6. The semiconductor-chip mounting substrate as set forth in claim 1, wherein a side of said first bump is a conductive-layer free surface, at which a side of said projection is exposed.

7. The semiconductor-chip mounting substrate as set forth in claim 1, wherein said substrate comprises a second projection as a stopper, which has a height of preventing the occurrence of an excessive contact pressure between said first bump and said second bump when said semiconductor chip is mounted on said substrate.

8. The semiconductor-chip mounting substrate as set forth in claim 1, wherein said substrate has a recess for receiving said second bump of said semiconductor chip in a top surface of said first bump.

9. The semiconductor-chip mounting substrate as set forth in claim 1, wherein one of said first bump and said second bump has a surface layer of a metal material selected from tin and tin alloys, the other one has a gold layer, and wherein the semiconductor-chip mounting substrate comprises a solid state diffusion layer of tin and gold formed at an interface between said first and second bumps.

10. The semiconductor-chip mounting substrate as set forth in claim 1, wherein the material of said substrate has an elastic modulus of 5 GPa or more.

11. The semiconductor-chip mounting substrate as set forth in claim 1, wherein said conductive layer includes a nickel layer having a thickness of 5 μm or more.

12. The semiconductor-chip mounting substrate as set forth in claim 2, wherein said at least one projection is a plurality of projections, and said substrate has a concave between adjacent projections, in which said resin material is filled.

13. The semiconductor-chip mounting substrate as set forth in claim 1, wherein said first bump is pressed against said second bump through a

cushion member of a metal material having a high plastic-deformation capability.

14. The semiconductor-chip mounting substrate as set forth in claim 1, wherein said first bump is of a tapered shape having a flat top end, and a value determined by dividing a height of said first bump by a diameter of a circle having substantially the same area as a base of said first bump is 0.5 or more.

15. The semiconductor-chip mounting substrate as set forth in claim 1,
wherein said substrate has a concave, in which said semiconductor chip can be incorporated,
said first bump is integrally molded at a bottom surface of said concave with said substrate,
said pressure holding means is a pressure holding member having a first surface adapted to contact a surface opposed to said second bump of said semiconductor chip, and a second surface extending around said first surface,
wherein the second surface of said pressure holding member is bonded to said substrate such that the first surface of said pressure holding member pushes said semiconductor chip placed in said concave toward said substrate, to thereby provide the required contact pressure between said first bump and said second bump.

16. The semiconductor-chip mounting substrate as set forth in claim 15, wherein said pressure holding member has a conductive film on at least said first surface, and a first metal film formed on said second surface so as to make an electrical connection with said conductive film, said substrate has a second metal film on a top surface around said concave, and

wherein the said pressure holding member is bonded to said substrate through an alloy layer generated at an interface between said first metal film and said second metal film.

17. The semiconductor-chip mounting substrate as set forth in claim 15, wherein said pressure holding member is bonded to said substrate such that an interior of said concave is sealed in air-tight manner.

18. The semiconductor-chip mounting substrate as set forth in claim 15, wherein said semiconductor chip is an optical element, and said pressure holding member has an aperture in the first surface, through which a transmission of light between said optical element placed in said concave and an outside of the semiconductor-chip mounting substrate becomes possible.

19. The semiconductor-chip mounting substrate as set forth in claim 15, wherein said semiconductor chip is an optical element, and said pressure

holding member has a window portion made of an optically transparent material, through which a transmission of light between said optical element placed in said concave and an outside of the semiconductor-chip mounting substrate becomes possible.

20. The semiconductor-chip mounting substrate as set forth in claim 15, wherein at least a part of said semiconductor-chip mounting substrate is encapsulated in a second substrate of a resin material, so that a shrinkage caused by curing of said resin material increases the contact pressure between said first bump and said second bump through said pressure holding member.

21. The semiconductor-chip mounting substrate as set forth in claim 20, wherein said semiconductor chip is an optical element, and said pressure holding member has a window portion made of an optically transparent material, said second substrate has an aperture, and

wherein a transmission of light between said optical element placed in said concave and an outside of the semiconductor-chip mounting substrate becomes possible through said window portion and said aperture.

22. A method of manufacturing a semiconductor-chip mounting substrate comprising the steps of:

providing a substrate having at least one projection thereon, which is

integrally molded with said substrate;

forming a conductive layer on said projection to obtain a first bump;

providing a semiconductor chip having a terminal projecting as a second bump on its surface;

pressing said second bump against said first bump under a pressure that is in an elastic deformation range of said first bump and causes a plastic deformation of said second bump, to bring the second bump into intimate contact with said first bump, and

providing a pressure holding means to hold a required contact pressure between said first bump and said second bump under the intimate contact condition.

23. The method as set forth in claim 22, wherein an intermediate assembly, which is composed of said semiconductor chip placed on said substrate such that said first bump contacts said second bump, and a thermosetting resin material filled as said pressure holding means in a space between said semiconductor chip and said substrate, is provided, said second bump is pressed against said first bump under a pressure that is within an elastic deformation range of said first bump and causes a plastic deformation of said second bump, to thereby bring the second bump into intimate contact with said first bump, and then the required contact pressure between said first bump and said second bump is held by curing said resin material in said intermediate assembly at a raised temperature under the intimate contact condition.

24. The method as set forth in claim 23, wherein said thermosetting resin material has a coefficient of linear expansion greater than a material of said substrate, and wherein said resin material in said intermediate assembly is cured at the raised temperature under the intimate contact condition, and a shrinkage caused by cooling of the cured resin material further increases the required contact pressure between said first bump and said second bump.

25. The method as set forth in claim 23, wherein said second bump is made of a solder material, and

wherein said resin material in said intermediate assembly is cured at the raised temperature lower than a melting point of said solder material, and then said intermediate assembly is heated at a temperature of the melting point of said solder material or more to carry out soldering between said first bump and said second bump.

26. The method as set forth in claim 23, wherein said resin material in said intermediate assembly is cured at the raised temperature, while applying ultrasonic to said intermediate assembly to carry out ultrasonic bonding between said first bump and said second bump.